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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/845,477	04/30/2001	Chine-Gie Lou	TS2000499	2319

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EXAMINER
GUERRERO, MARIA F

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/845,477	LOU, CHINE-GIE	
	Examiner	Art Unit	
	Maria Guerrero	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is the first action on the merits.

Claims 1-24 are pending.

Specification

2. The abstract of the disclosure is objected to because exceed 150 words in length. Correction is required. See MPEP § 608.01(b).

The disclosure is objected to because of the following informalities: the silicon nitride formula "Si_3N_4" is incorrect, in page 21, line 2.

Appropriate correction is required.

Claim Objections

3. Claims 1-23 are objected to because of the following informalities: claims 1 and 13 recite, "Creating reacted and unreacted salicide material". Claims 1, 12, and 13 recite the expression "adequate thickness". The term "unreacted" is misspelled in claim 12, lines 24, 26. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pey et al. (U.S. 6,180,501) in view of Givens et al. (U.S. 5,268,330).

Pey et al. teaches providing a semiconductor substrate having: a gate electrode (a pad oxide layer and a polysilicon layer) with gate spacers, shallow trench isolation regions, source and drain regions, and LDD regions (Fig. 1-7, col. 5, lines 1-60). Pey et al. discloses forming an etch stop material (silicon nitride) over the surface of the substrate (col. 5, lines 30-35). Pey et al. teaches forming a salicide layer by depositing a Ti/TiN layer (280 to 350 angstroms) over the surface of the substrate, including the surface of the gate spacers, and performing a first RTP anneal at a temperature of about 720-750 degrees C. for about 20 to 60 seconds (col. 5, lines 60-67, col. 6, lines 1-10). Pey et al. discloses creating a layer of titanium silicide over the surface of the source and drain regions, and removing the unreacted Ti/TiN layer by a selective wet etch (col. 6, lines 5-15). Pey et al. shows depositing a layer of dielectric (BPSG) over the surface of the layer of etch stop material, polishing the surface of the layer of dielectric down to the surface of the etch stop material, and removing the layer of etch stop material by plasma etching or RIE (col. 5, lines 35-40, col. 6, lines 23-50). Pey et al. teaches depositing a Ti/TiN layer over the surface of the polished layer of dielectric including the exposed surface of the polysilicon layer and performing a second anneal (col. 7, lines 55-60). Furthermore, Pey et al. teaches creating reacted salicide material over the surface of polysilicon, removing the unreacted material, and performing a third RTP anneal at 850°C for about 10 to 30 seconds (col. 6, lines 5-15, col. 7, lines 55-60).

Pey et al. fails to show depositing the etch stop material over the surface of the substrate including the gate spacers. However, Givens et al. shows forming the etch stop layer (silicon nitride) over the surface of the substrate including the gate spacers

(Fig. 2, col. 3, lines 50-68). Givens et al. teaches forming a dielectric layer over the etch stop layer and polishing the dielectric layer (Fig. 3, col. 4, lines 1-20).

Therefore, it would have been obvious to a person of ordinary skill in the art to include the formation of the etch stop layer over the gate spacers as taught Givens et al. in order to control the polishing of the dielectric layer (Givens et al., col. 3, lines 60-67).

Regarding the claimed thickness, temperature, and time, a particular parameter must first be recognized as a result-effective variable, i.e., a variable, which achieves a recognized result, before the determination of the optimum or workable ranges of, said variable might be characterized as routine experimentation. In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977). In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). In re Geisler, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

5. Claims 1, 3, 5, 9, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pey et al. (U.S. 6,153,485) (cited by Applicant) in view of Givens et al. (U.S. 5,268,330).

Pey et al. teaches a method for fabricating transistor having low sheet resistance gate electrodes (col. 1, lines 10-15). Pey et al. shows providing a semiconductor substrate having: a gate electrode (a pad oxide layer and a polysilicon layer) with gate spacers, shallow trench isolation regions, source and drain regions, and LDD regions (Fig. 1, col. 4, lines 35-67). Pey et al. teaches forming a salicide layer by depositing a metal layer over the surface of the substrate, including the surface of the gate spacers and performing a first rapid thermal anneal at a temperature between about 650° and 740° C. for about 20 to 40 seconds (Fig. 1, col. 5, lines10-25). Pey et al. discloses

creating reacted salicide material over the surface of the source and drain regions, and removing the unreacted metal layer (col. 5, lines 14-25).

Pey et al. shows forming an etch stop material over the surface of the substrate, depositing a layer of dielectric over the surface of the layer of etch stop material, polishing the surface of the layer of dielectric down to the surface of the etch stop material, and removing the layer of etch stop material (Fig. 2-4A, col. 5, lines 32-65, col. 6, lines 10-12). Pey et al. teaches depositing a metal layer over the surface of the polished layer of dielectric including the exposed surface of the polysilicon layer and performing a second anneal (col. 6, lines 32-46). Furthermore, Pey et al. teaches creating reacted salicide material over the surface of polysilicon, removing the unreacted material, and performing a third rapid thermal anneal at a temperature range of between about 700° to 900° C. for about 20 to 40 seconds (Fig. 5, col. 6, lines 40-46).

Pey et al. fails to show depositing the etch stop material over the surface of the substrate including the gate spacers. However, Givens et al. shows forming the etch stop layer (silicon nitride) over the surface of the substrate including the gate spacers (Fig. 2, col. 3, lines 50-68). Givens et al. teaches forming a dielectric layer over the etch stop layer and polishing the dielectric layer (Fig. 3, col. 4, lines 1-20).

Therefore, it would have been obvious to a person of ordinary skill in the art to include the formation of the etch stop layer over the gate spacers as taught Givens et al. in order to avoid over etching of the polysilicon layer.

Regarding the claimed thickness, temperature, and time, a particular parameter must first be recognized as a result-effective variable, i.e., a variable, which achieves a

recognized result, before the determination of the optimum or workable ranges of, said variable might be characterized as routine experimentation. In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977). In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). In re Geisler, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

6. Claims 13-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pey et al. (U.S. 6,180,501) in view of McAnally et al. (U.S. 6,136,700).

Pey et al. teaches providing a semiconductor substrate having: a gate electrode (a pad oxide layer and a polysilicon layer) with gate spacers, shallow trench isolation regions, source and drain regions, and LDD regions (Fig. 1-7, col. 5, lines 1-60). Pey et al. discloses forming an etch stop material (silicon nitride) over the surface of the substrate and patterning the pad oxide layer, the polysilicon layer, and the etch stop material (Fig. 1-2, col. 5, lines 1-15).

Pey et al. teaches forming a salicide layer by depositing a Ti/TiN layer (280 to 350 angstroms) over the surface of the substrate, including the surface of the gate spacers, and performing a first RTP anneal (col. 5, lines 60-67, col. 6, lines 1-10). Pey et al. discloses creating a layer of titanium silicide over the surface of the source and drain regions, and removing the unreacted Ti/TiN layer (col. 6, lines 5-15). Pey et al. shows depositing a layer of dielectric (BPSG) over the surface of the layer of etch stop material, polishing the surface of the layer of dielectric down to the surface of the etch stop material, and removing the layer of etch stop material (col. 6, lines 23-50).

Pey et al. teaches depositing a Ti/TiN layer over the surface of the polished layer of dielectric including the exposed surface of the polysilicon layer and performing a second anneal (col. 7, lines 55-60). Furthermore, Pey et al. teaches creating reacted salicide material over the surface of polysilicon, removing the unreacted material, and performing a third RTP anneal at 850°C for about 10 to 30 seconds (col. 6, lines 5-15, col. 7, lines 55-60).

Pey et al. fails to show using a boronitride layer. However, McAnally et al. shows using a boronitride layer as a stopping layer in order to increase the etch selectivity (col. 3, lines 17-25, col. 4, lines 15-20, col. 5, lines 25-30).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Pey et al.'s process by using boronitride instead of silicon nitride as taught McAnally et al. The modification would reduce the possibility of a short between the polysilicon and the subsequently formed silicide layer (McAnally et al., col. 5, lines 32-38).

Regarding the claimed thickness, temperature, and time, a particular parameter must first be recognized as a result-effective variable, i.e., a variable, which achieves a recognized result, before the determination of the optimum or workable ranges of, said variable might be characterized as routine experimentation. In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977). In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). In re Geisler, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Poon et al. (U.S. 5,064,683) teaches using a boron nitride polish stop. Stanley Wolf "Silicon Processing for the VLSI Era" teaches, as well known in the art, rapid thermal processing at 600-800°C to form a silicide layer, selectively removed the unreacted Ti, annealing the titanium silicide at temperature of 1000°C. for 30 seconds to reduce the titanium silicide resistivity (page 148). Buynoski (U.S. 6,187,675 and Huster et al. (U.S. 6,391,767) teach a silicide process to reduce gate resistance.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 703-305-0162.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MG
June 14, 2002

CARL WHITEHEAD, JR.
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